DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128160A CCH-PW-N

Product Specification ***Version: 1.1.1***

30.09.2008

GENERAL SPECIFICATION

MODULE NO. :

DEM 128160A CCH-PW-N

CUSTOMER

VERSION NO.	CHANGE DESCRIPTION	DATE
0	ORIGINAL VERSION	02.02.2005
1	CHANGED DIMENSIONS	26.07.2006
1.1.1	CHANGED IC	30.09.2008

PREPARED BY: ZXD DATE: 30.09.2008

APPROVED BY: MH DATE: 13.10.2008

CONTENTS

1. FUNCTIONS &FEATURES

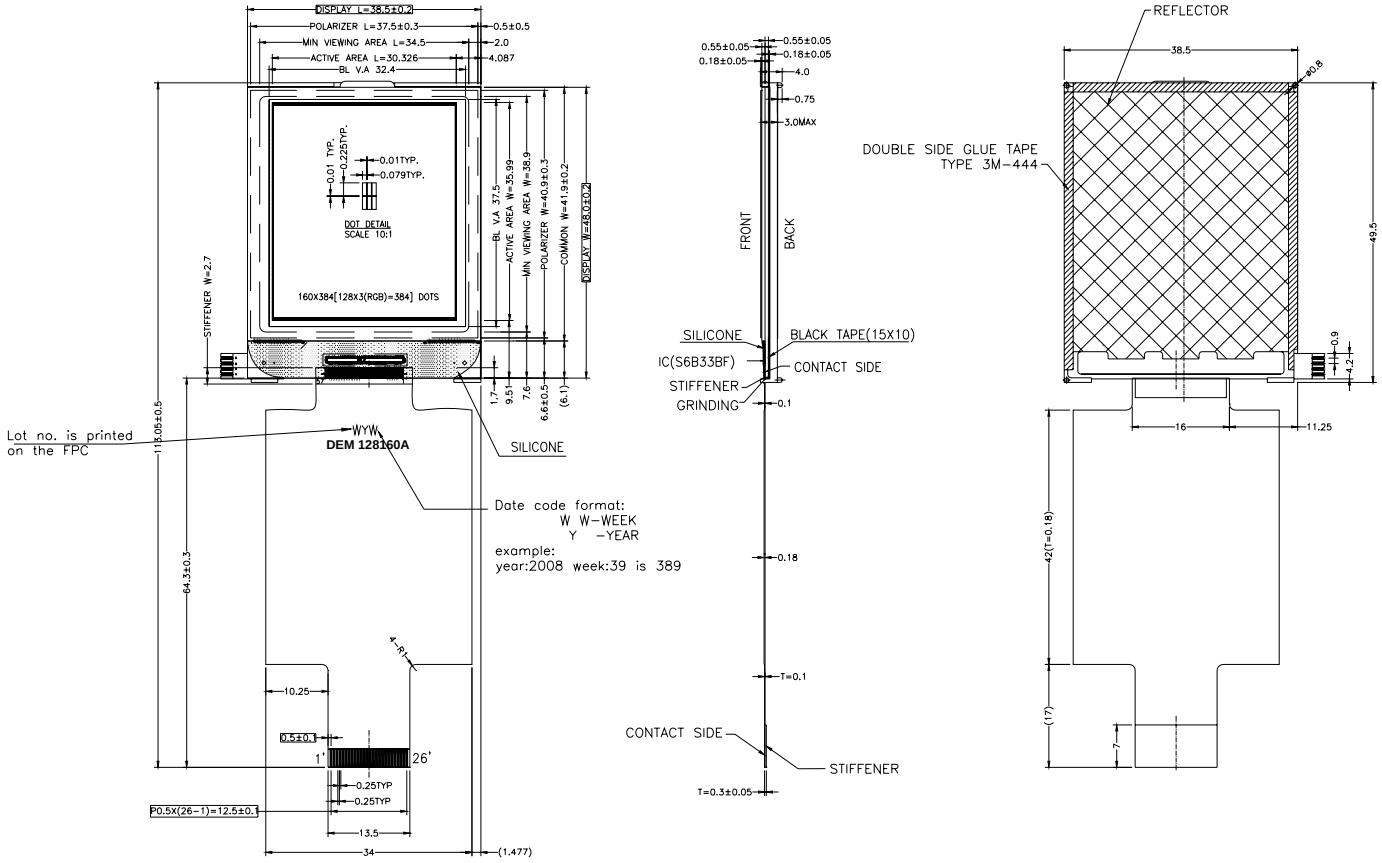
MODULE NAME	LCD TYPE	BACKLIGHT
DEM 128160A CCH-PW-N	Color-STN Transmissive Negative Mode	LED, Lightguide, White

- Display Size : 1,9" C-STN (Colour-STN)
- Display Colour : 65k Colours
- IC Type : S6B33BF (Samsung)
- Viewing Direction : 6 o'clock
- Driving Scheme : 1/162 Duty, 1/7Bias
- Power Supply Voltage : 3.0 Volt (typ.)
- Lcd Voltage : 10.6 Volt (typ.)
- Operating Temperature : -20°C to 70°C
- Storage Temperature : -30ºC to 80°C

2. MODULE ARTWORK

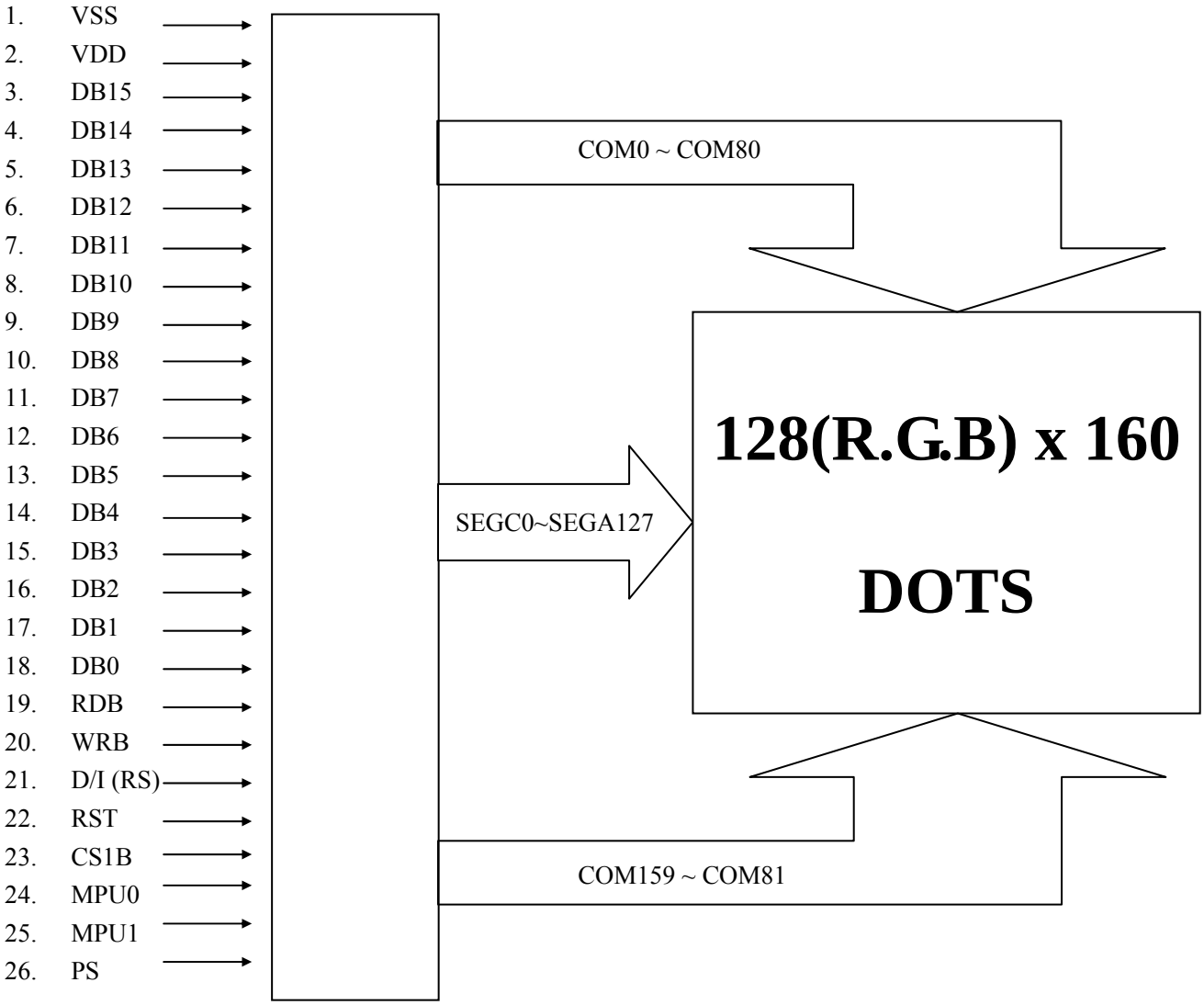
- Module Size : 38.50 x 113.05 x 3.0 mm
- Viewing Area : 34.50 x 38.90 mm
- Dot Number : 128(RGB) x 160

3. EXTERNAL DIMENSIONS



Remarks:
1.Unmarked tolerance is ±0.25
2.All materials comply with RoHs.

4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

<table>
<tr><th>Pin NO.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>Vss</td><td>Ground</td></tr>
<tr><td>2</td><td>Vdd</td><td>Power supply</td></tr>
<tr><td>3~18</td><td>DB[15:8]
DB[7]/SDI
DB[6]/SCL
DB[5:0]</td><td>-DB[15:0]: 16-bit bi-directional data bus.
-SDI: Serial data input pin. The data is latched at the rising edge of SCL.
-SCL: Serial clock input pin.</td></tr>
<tr><td>19</td><td>RDB
(E)</td><td>Read / Write execution control pin
<table>
<tr><th>MPU[1]</th><th>MPU Type</th><th>RDB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
− R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.
− R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin When RDB is “L”, DB0 to DB15 are in an output status.</td></tr>
</table></td></tr>
<tr><td>20</td><td>WRB
(R/W)</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
− R/W = “H”: read
− R/W = “L”: write</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin The data on DB0 to DB15 are latched at the rising edge of the WRB signal.</td></tr>
</table></td></tr>
<tr><td>21</td><td>D/I
(RS)</td><td>Data / Instruction select input pin
− D/I = “H”: DB0 to DB15 are display data
− D/I = “L”: DB0 to DB7 are instruction data</td></tr>
<tr><td>22</td><td>RSTB</td><td>Reset input pin. When RSTB is “L”, initialization is executed.</td></tr>
<tr><td>23</td><td>CS1B</td><td>Chip select input pins Data / instruction I/O is enabled only when CS1B is “L”. When chip select is non-active, DB0 to DB15 may be high impedance.</td></tr>
<tr><td>24~26</td><td>PS
MPU[1:0]</td><td>MPU interface select pin
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU[0]</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>8080-series 8bit interface</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>8080-series 16bit interface</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>6800-series 8bit interface</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>6800-series 16bit interface</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>3 pin SPI(Write only)</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>4 pin SPI(Write only)</td></tr>
</table></td></tr>
</table>

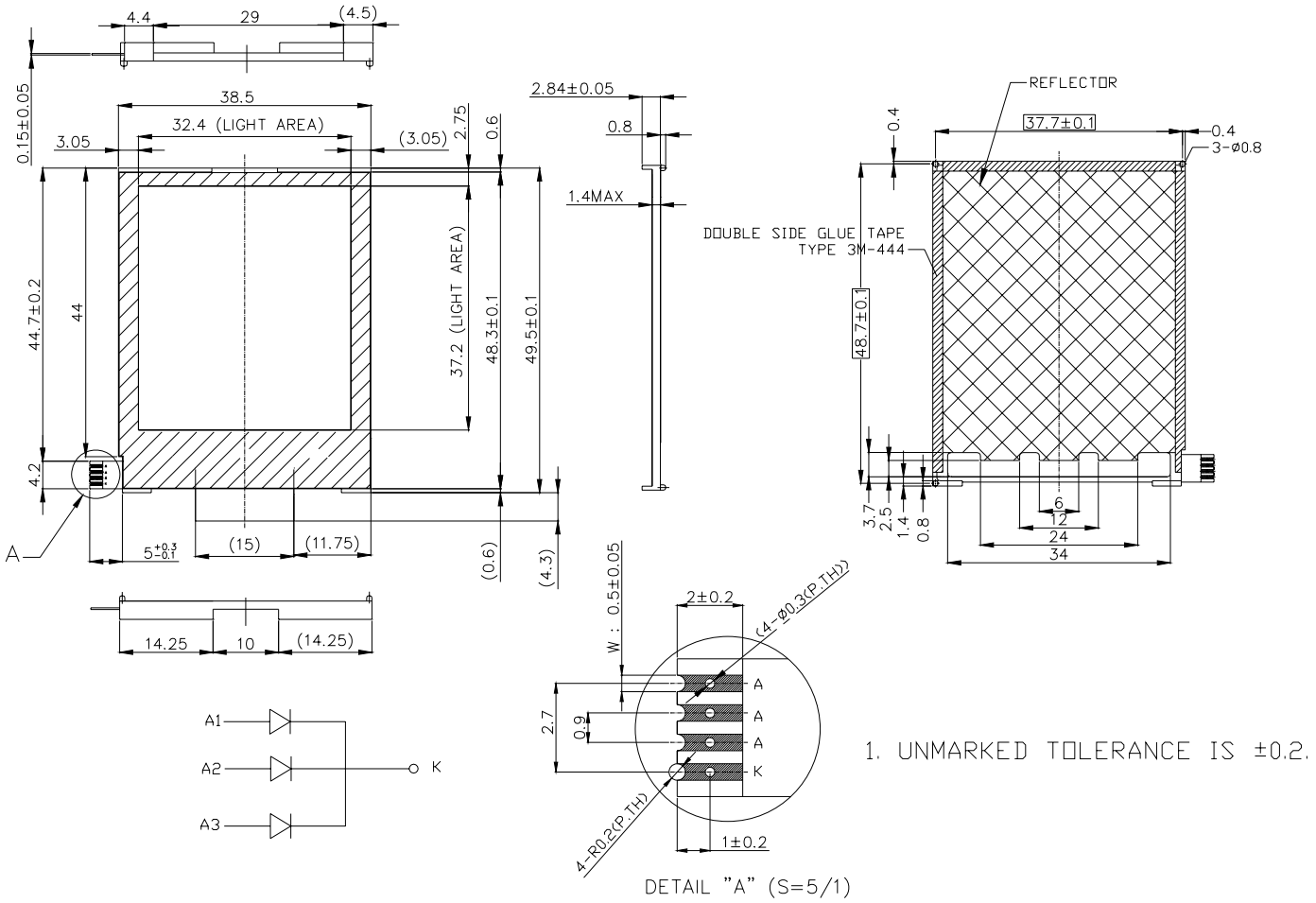
6. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATIONS

Electronics/Optical Specifications:

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	Vf		3.3		V	If= 45 mA
Forward Current	If		45	60	mA	
Power Dissipation	Pd		0.15		W	If= 45 mA
Reverse Voltage	VR		5.0		V	
Reverse Current	IR		0.3		mA	VR = 5 V
Luminous Intensity	Iv		2000		cd/m^2	If= 45 mA
Luminous Uniformity		80			%	If= 45 mA
Color Chromaticity	X	0.275		0.330		If=15mA Ta=25°C Each chip
	Y	0.270		0.339		

	SYMBOL	RATINGS
Operating Temperature	Topr	−30°C to +70°C
	Tsty	−40°C to +80°C

Operating life time: Longer than 50000 hours



7. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage range	VDD3	-0.3 to +4.0	V
	VDD	-0.3 to +2.3	
	VIN1	-0.3 to +4.0	
LCD Supply Voltage range	|VCC – VEE|	22	V
Input Voltage range	Vin	- 0.3 to VDD3 +0.3	V
Operating Temperature range	TOPR	-20 to +70	°C
Storage Temperature range	TSTR	-30 to +80	°C

8. DC CHARACTERISTICS

8.1 DC CHARACTERISTICS

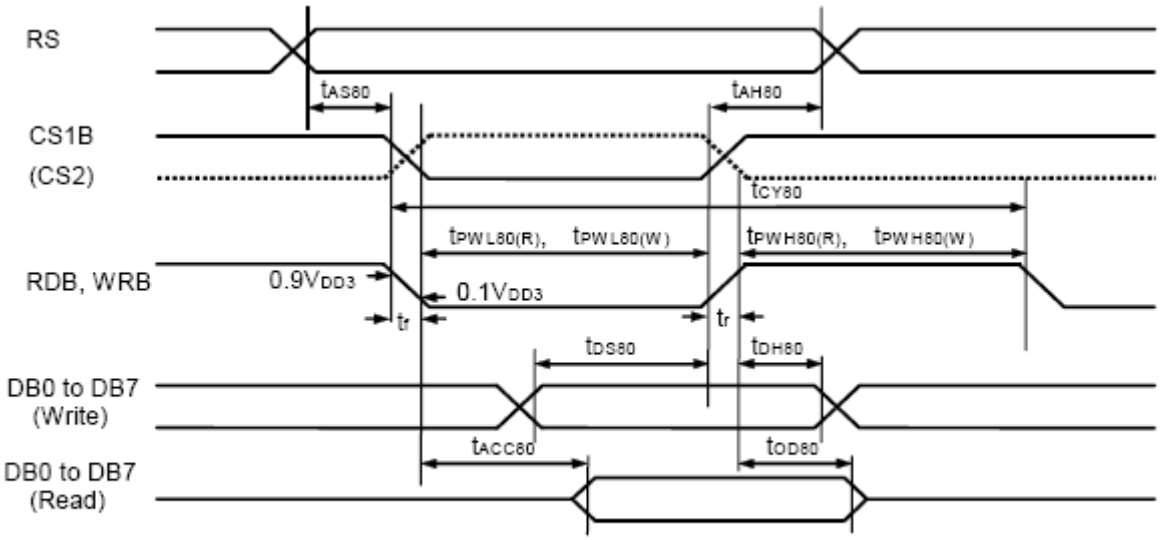
(Vss = 0V, VDD3 = 1.65 to 3.3V, Ta = -20 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Operating voltage		VDD3		1.65		3.3	V	VDD3
Operating voltage		VDD		1.45		1.55	V	VDD
Operating voltage		VIN1		2.4	-	3.6	V	VIN1,VIN1A
Operating voltage		VIN2		2.4	-	5.5	V	
Operating voltage		VIN45		2.4	-	5.5	V	VOUT45
Operating voltage		DC2IN	1/7 Bias	2.0	-	4.0	V	DC2OUT
Operating voltage		2Vr	2Vr = |(VRP) - (VRN)|	4.0	-	20	V	VRP, VRN
Output voltage		VREG	REG_OUT voltage	1.5 ± 0.05			V	VREG
Driving voltage input range		VM	External power supply mode	1.0		2.0	V	VMOUT
		VCC		5.0		12.0	V	VRP
		VEE		-3.0		-8.0	V	VRN
Input voltage	High	VIH		0.8VDD3	-	VDD3	V	
	Low	VIL		VSS	-	0.2VDD3		
Output voltage	High	VOH	IOH = 0.5mA	0.8VDD3	-	VDD3	V	
	Low	VOL	IOL = 0.5mA	VSS	-	0.2VDD3		
Oscillator Frequency Tolerance	Normal or Partial 0	FOSC1	(*R1)=72k Ohm, (fFR=80Hz target), DSG=0, 162 Duty, VDDO=1.5V, Ta=25°C	253.4	281.6	309.7	kHz	OSC1OSC2 -
	Partial 1	FOSC2	DSG=0, 66 Duty VDDO=1.5V, Ta=25°C	84.46	93.86	103.23	kHz	fOSC1/3
Driving voltage input range		V1 VM		2.0 1.0	-	4.0 2.0	V	
Regulator output range		REG_OUT	RTEST = "L"	1.45	1.5	1.55	V	

Note : (*R1),(*R2) resistances are only recommended to get target frame frequency. But the value is not absolute.

9. AC CHARACTERISTICS

9-1. Read / Write Characteristics (8080-series MPU)



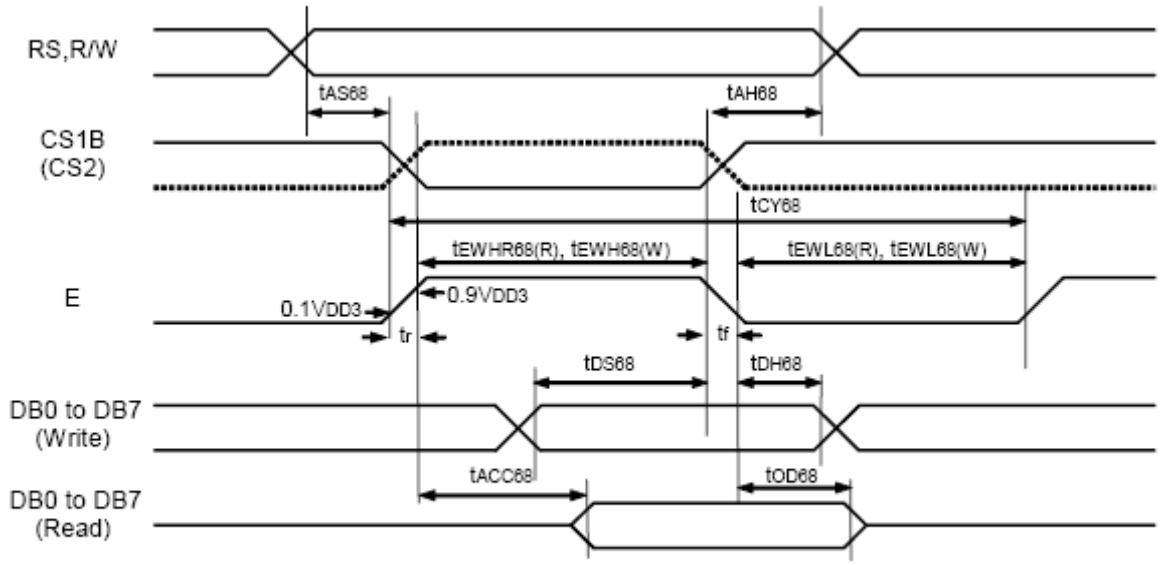
** tPWL80(W) and tPWL80(R) is specified in the overlapped period when CS1B is low (CS2 is high) and WRB(RDB) is low.
** The difference between transition time for rising/falling of the input signals(RS,CS1B,CS2,RDB,WRB) should be less than 2ns.

(V_{DD3} = 1.65 to 3.3V, Ta = -20 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	RS	tAS80 tAH80		0 0		ns
System cycle time(For write)		tCY80		100		ns
Pulse width low for write Pulse width High for write	WRB (WRB)	tPWL80(W) tPWH80(W)		40 40		ns
Pulse width low for read Pulse width high for read	RDB (RDB)	tPWL80(R) tPWH80(R)		120 40		ns
Data setup time Data hold time	DB0 to DB15	tDS80 tDH80		10 10		ns
Read access time		tACC80	CL = 50 pF		150	ns
Output disable time		tOD80	no load	20		ns

NOTE: *1. (tr + tf) < (tCY80 – tPWL80(W) – tPWH80(W)) for write, (tr + tf) < (tCY80 – tPWLR80 – tPWHR80) for read.

9-2. Read / Write Characteristics (6800-series Microprocessor)



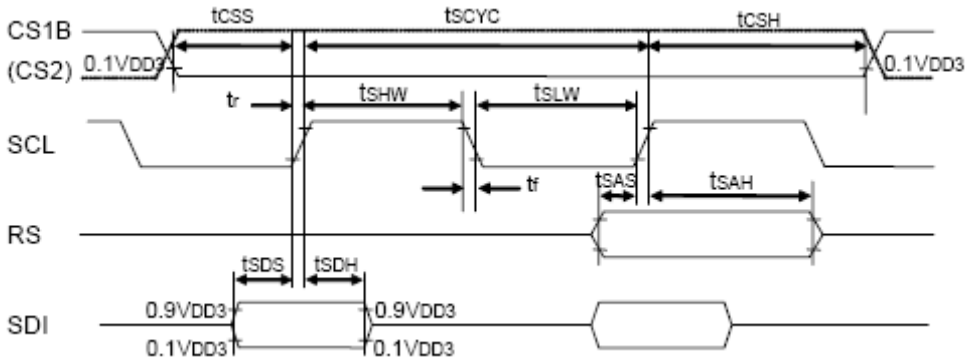
** tEWH68(W) and tEWH68(R) is specified in the overlapped period when CS1B is low (CS2 is high) and E is high.
** The difference between transition time for rising/falling of the input signals(RS,R/W,CS1B,CS2,E) should be less than 2ns.

(V_{DD3} = 1.65 to 3.3V, Ta = -20 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	RS, WRB (R/W)	tAS68 tAH68		0 0		ns
System cycle time(For write)		tCY68		100		ns
Enable width high for write Enable width low for write	RDB (E)	tEWH68(W) tEWL68(W)		40 40		ns
Enable width high for read Enable width low for read	RDB (E)	tEWH68(R) tEWL68(R)		120 40		ns
Data setup time Data hold time	DB0 to DB15	tDS68 tDH68		10 10		ns
Read access time		tACC68	CL = 50 pF		150	ns
Output disable time		tOD68	no load	20		ns

NOTE: *1. (tr + tf) < (tCY68 – tEWH68(W) – tEWL68(W)) for write, (tr + tf) < (tCY68 – tEWH68(R) – tEWL68(R)) for read.

9-3. Serial Data Interface (4 PIN) Timing

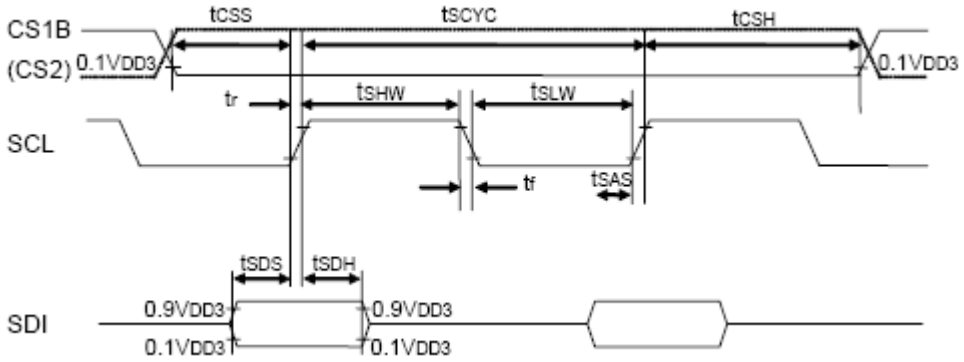


(V_{DD3} = 1.65 to 3.3V, Ta = -20 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	tSCYC		75	ns
SCL High Pulse Width	SCL	tSHW		20	ns
SCL Low Pulse Width	SCL	tSLW		20	ns
SDI Setup time	SDI	tSDS		10	ns
SDI Hold time	SDI	tSDH		10	ns
RS Setup time	RS	tSAS		10	ns
RS Hold time	RS	tSAH		10	ns
Chip Select Setup time	CS1B (CS2)	tCSS		10	ns
Chip Select Hold time	CS1B (CS2)	tCSH		0	ns

NOTE: *1. (tr + tf) < (tSCYC – tSHW – tSLW) for write.

9-4. Serial Data Interface (3 PIN) Timing

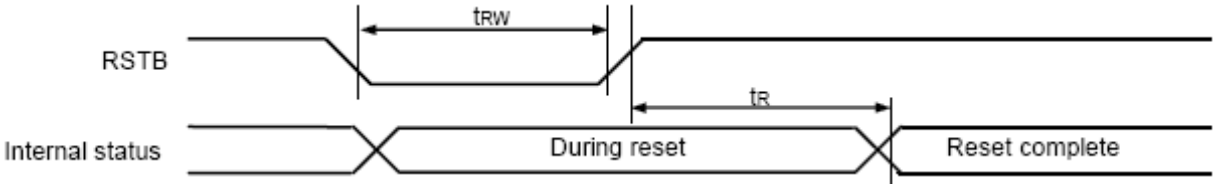


(V_{DD3} = 1.65 to 3.3V, Ta = -20 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	tSCYC		75	ns
SCL High Pulse Width	SCL	tSHW		20	ns
SCL Low Pulse Width	SCL	tSLW		20	ns
SDI Setup time	SDI	tSDS		10	ns
SDI Hold time	SDI	tSDH		10	ns
Chip Select Setup time	CS1B (CS2)	tCSS		10	ns
Chip Select Hold time	CS1B (CS2)	tCSH		0	ns

NOTE: *1. (tr + tf) < (tSCYC – tSHW – tSLW) for write.

9-5. Reset Input Timing



(V_{DD3} = 1.65 to 3.3V, Ta = -20 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RSTB	TRW		1000	-	ns
Reset time	-	tR		-	1000	ns

10. LCD MODULES HANDLING PRECAUTIONS

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

11. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections.