

TLE4961-5K

High Precision Automotive Hall Effect Latch

Technical Product Description

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Preliminary Information

1 Product Description



1.1 Overview

The TLE4961-5 is a high precision Hall effect switch with a latching characteristic, highly accurate switching thresholds for operating temperatures up to 170°C.



Figure 1-1 Image of TLE4961-5 in the PG-SC59-3-5 package

1.2 Features

- 3.0V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent and overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 1µs)
- High ESD performance
- SOT23 like SMD package PG-SC59-3-5

1.3 Target Applications

Target applications for the TLE496x Hall switch family are all applications which require a high precision Hall latch with a operating temperature range from -40°C to 170°C. Its superior supply voltage range from 3.0 V to 32V with overvoltage capability (e.g. load-dump) up to 42 V without external resistor make it ideally suited for automotive and industrial applications.

The TLE4961-5K is a latch with a typical threshold of 15mT. It is ideally suited for applications with a pole wheel for index counting and speed measurement.

Table 1-1 Ordering Information

Product Name	Product Type	Ordering Code	Package
TLE4961-5K	Hall Latch	SP000910192	PG-SC59-3-5

2 Functional Description

2.1 General

The TLE4961-5 is an integrated Hall effect latch designed specifically for highly accurate applications with superior supply voltage capability, operating temperature range and temperature stability of the magnetic thresholds.

2.2 Pin Configuration (top view)

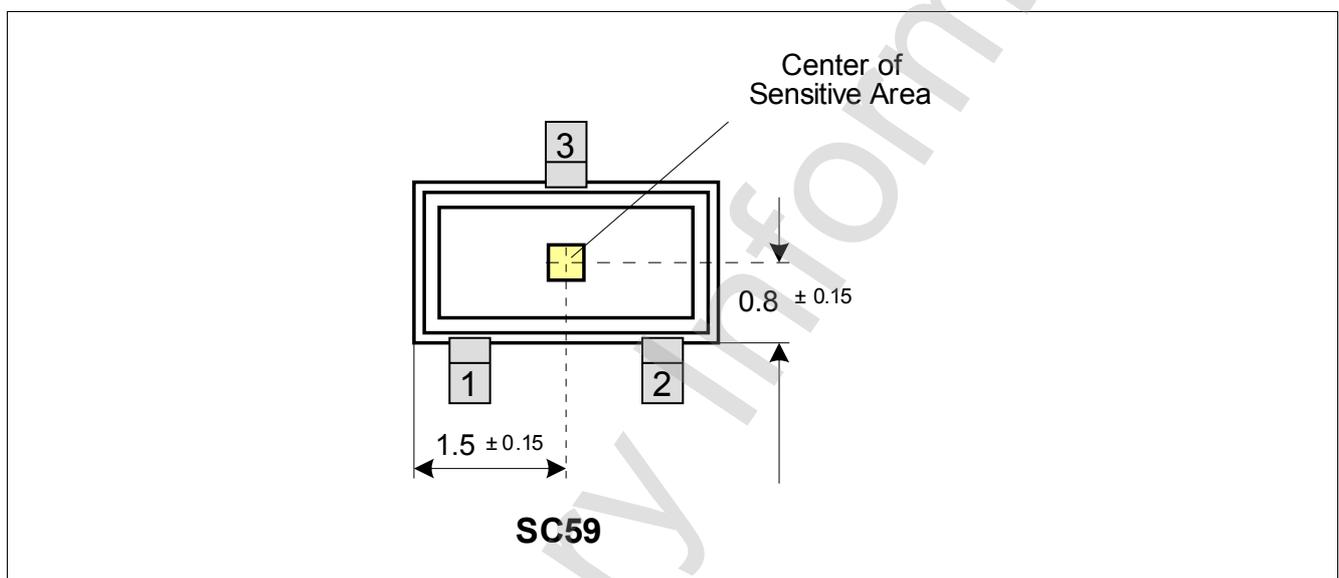


Figure 2-1 Pin Configuration and Center of Sensitive Area

2.3 Pin Description

Table 2-1 Pin Description PG-SC59-3-5

Pin No.	Symbol	Function
1	V_{DD}	Supply voltage
2	Q	Output
3	GND	Ground

2.4 Block Diagram

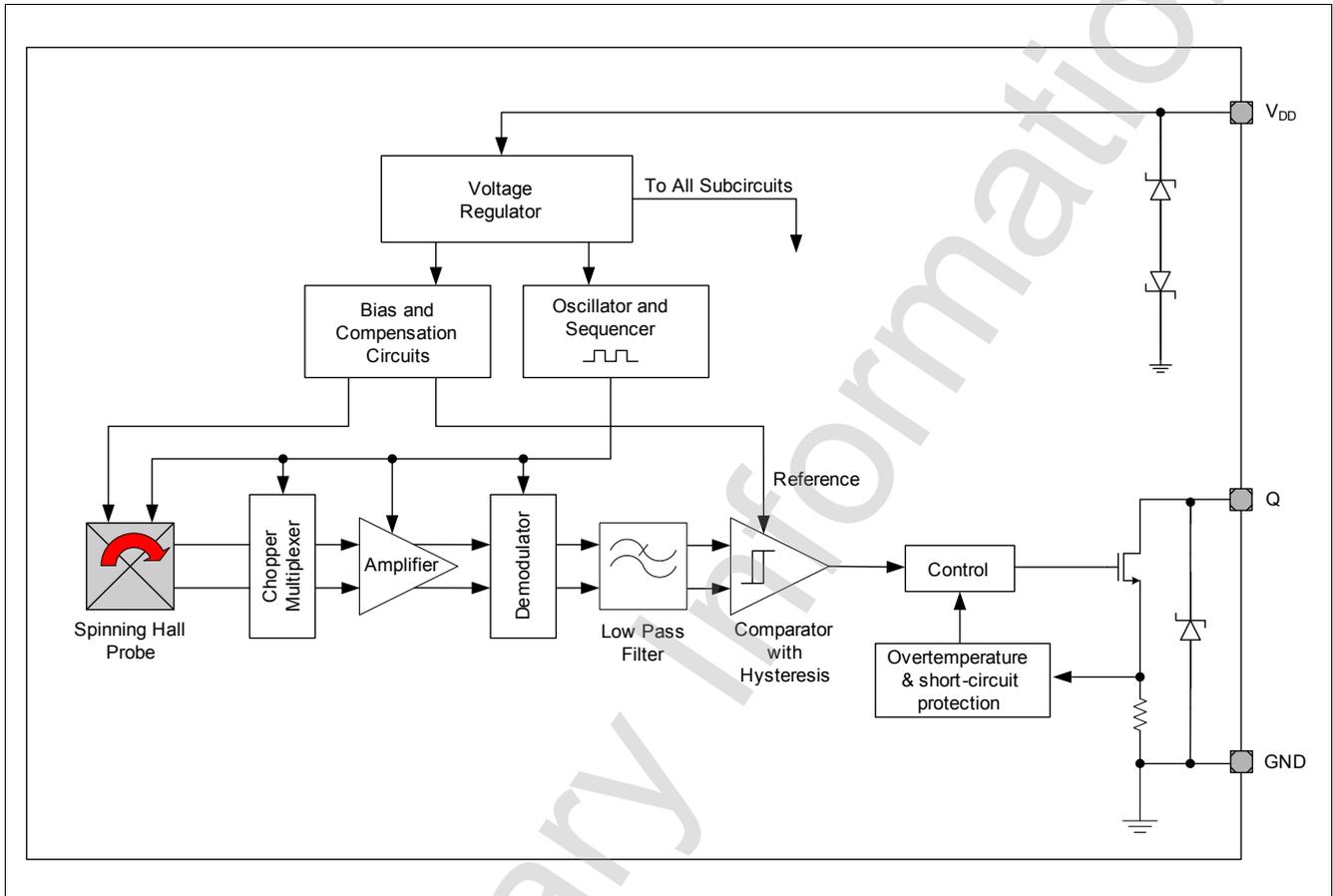


Figure 2-2 Functional Block Diagram TLE4961-5

2.5 Functional Block Description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

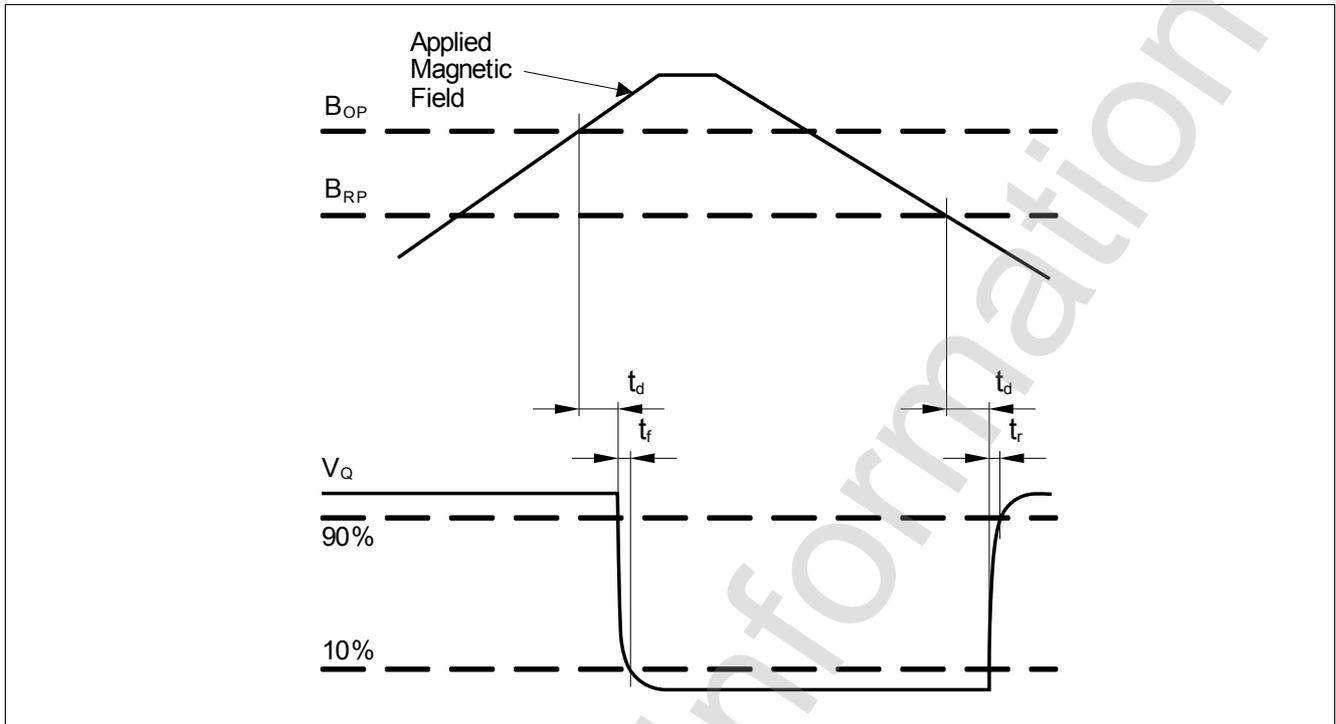


Figure 2-3 Timing Diagram TLE4961-5

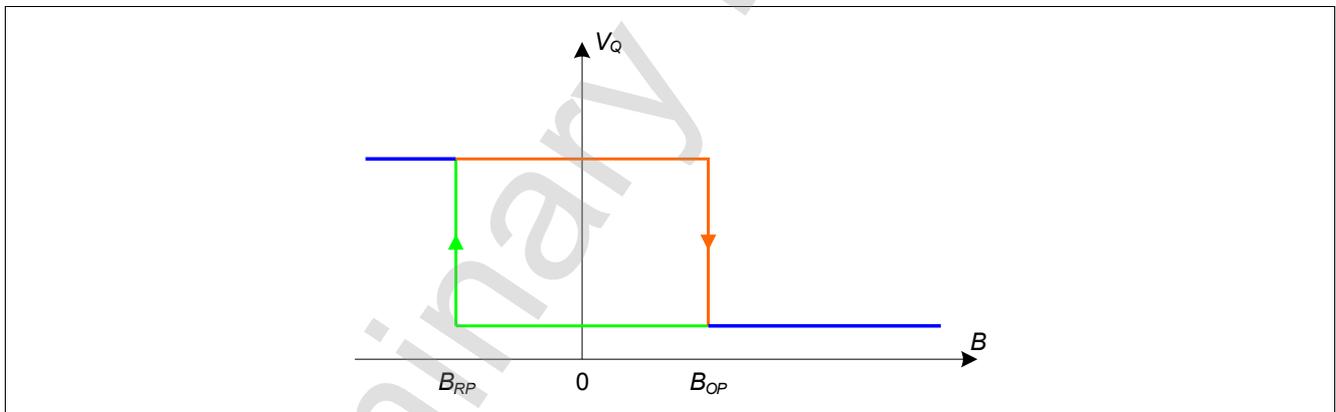


Figure 2-4 Output Signal TLE4961-5

3 Specification

3.1 Application Circuit

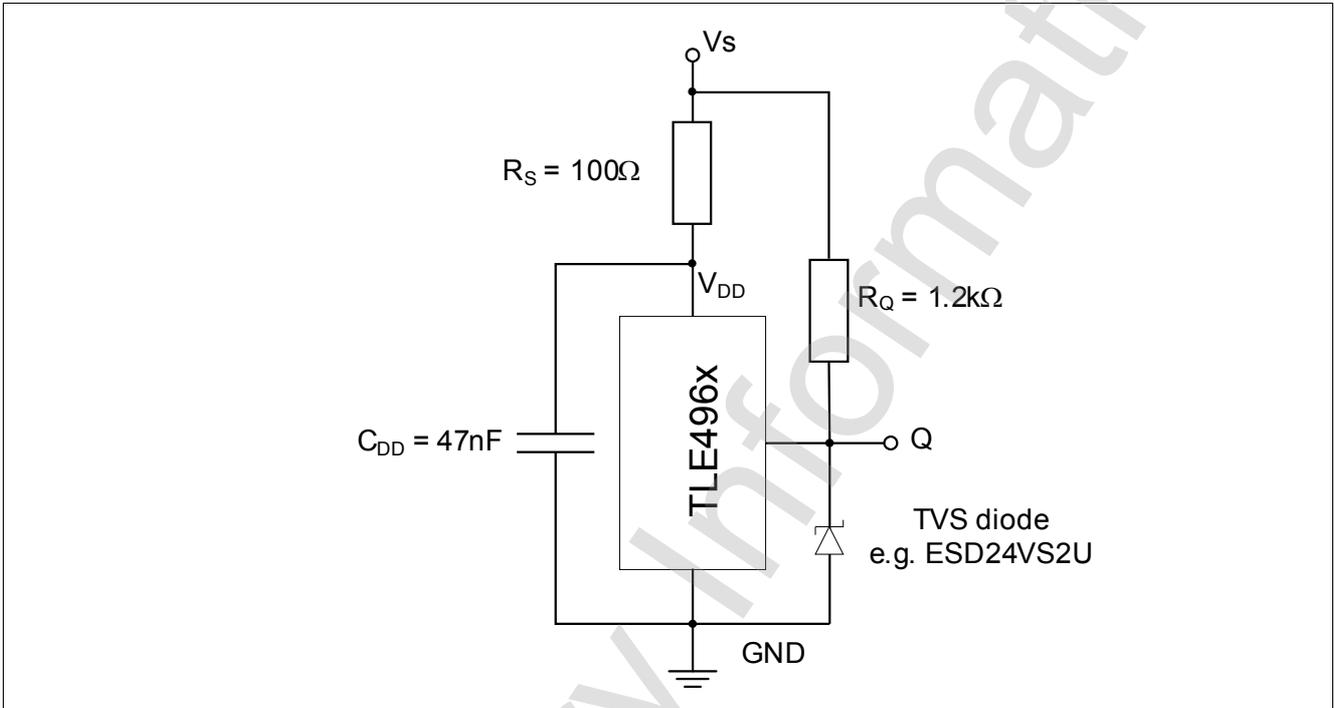


Figure 3-1 Application Circuit 1: with external resistor

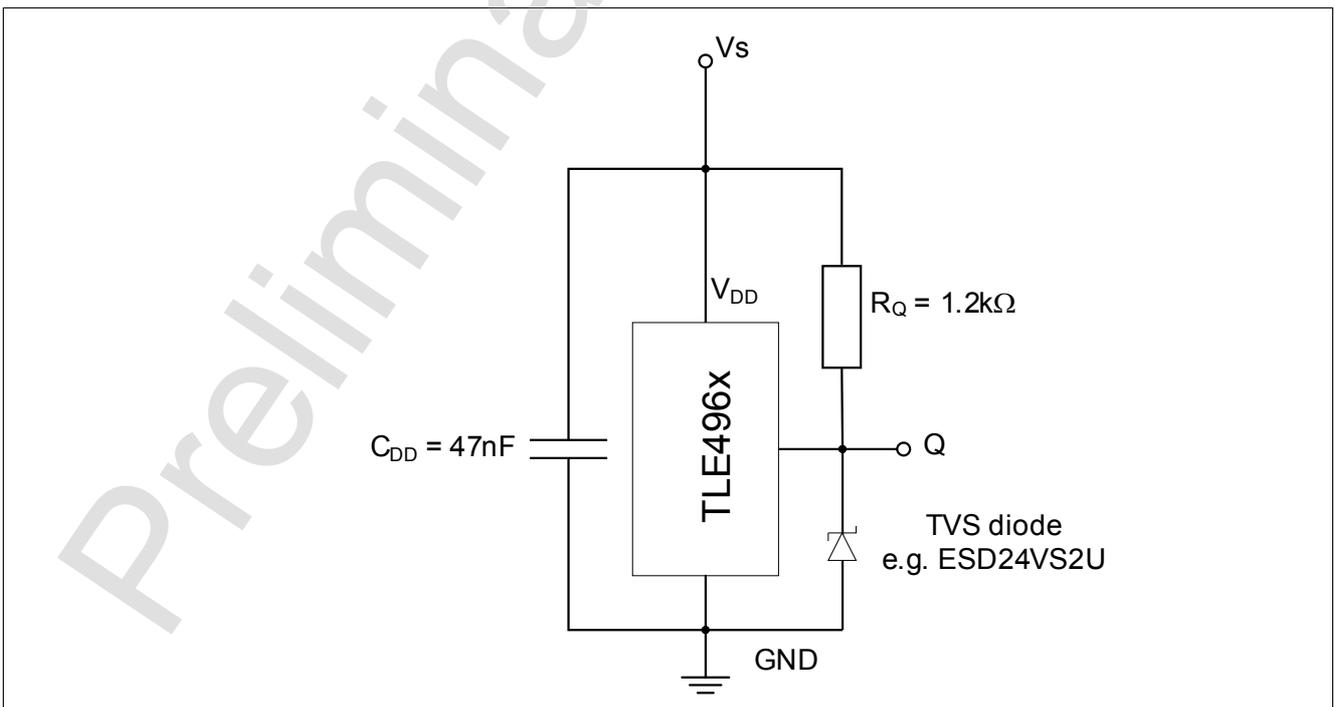


Figure 3-2 Application Circuit 2: without external resistor

3.2 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
Supply voltage	V_{DD}	-18	32 42	V	10h, no external resistor required
Output voltage	V_Q	-0.7	32	V	
Reverse output current	I_Q	-70		mA	
Junction temperature	T_J	-40	155 165 175 195	°C	for 2000h (not additive) for 1000h (not additive) for 168h (not additive) for 3 x 1h (additive)
Thermal resistance junction ambient	R_{thJA}		300	K/W	for PG-SC59-3-5
Thermal resistance junction lead	R_{thJL}		100	K/W	for PG-SC59-3-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power P_{DIS} and junction temperature T_J of the chip (SC59 example):

e.g for: $V_{DD} = 12\text{ V}$, $I_S = 2.5\text{ mA}$, $V_{QSAT} = 0.5\text{ V}$, $I_Q = 20\text{ mA}$
 Power dissipation: $P_{DIS} = 12\text{ V} \times 2.5\text{ mA} + 0.5\text{ V} \times 20\text{ mA} = 30\text{ mW} + 10\text{ mW} = 40\text{ mW}$
 Temperature $\Delta T = R_{thJA} \times P_{DIS} = 300\text{ K/W} \times 40\text{ mW} = 12\text{ K}$
 For $T_A = 150^\circ\text{C}$: $T_J = T_A + \Delta T = 150^\circ\text{C} + 12\text{ K} = 162^\circ\text{C}$

Table 3-2 ESD Protection¹⁾ ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
ESD voltage (HBM) ²⁾	V_{ESD}	± 7		kV	R = 1.5k Ω , C = 100pF
ESD voltage (SDM) ³⁾		± 1			
ESD voltage (system level) ⁴⁾		± 15			

- 1) Characterization of ESD is carried out on a sample basis.
- 2) Human Body Model (HBM) tests according to EIA/JESD22-A114
- 3) Socket device model (SDM) tests according to EOS/ESD-DS5.3-1993
- 4) Gun test (2k Ω / 330pF or 330 Ω / 150pF) according to ISO 10605-2008

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4961-5. All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

Table 3-3 Operating Conditions Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Supply voltage	V_{DD}	3.0	32 ¹⁾	V	
Output voltage	V_Q	-0.7	32	V	
Junction temperature	T_j	-40	170	°C	
Output current	I_Q	0	25	mA	
Magnetic signal input frequency ²⁾	f_{SW}	0	10	kHz	

- 1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.
- 2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3dB corner frequency of the internal low-pass filter in the signal path.

3.4 Electrical and Magnetic Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to $V_{DD} = 12\text{ V}$ and $T_A = 25^\circ\text{C}$. The below listed specification is valid in combination with the application circuit shown in [Figure 3-1](#) and [Figure 3-2](#)

Table 3-4 General Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_S	1.1	1.6	2.5	mA	
Reverse current	I_{SR}		0.05	1	mA	for $V_{DD} = -18\text{V}$
Output saturation voltage	V_{QSAT}		0.2	0.5	V	$I_Q = 20\text{mA}$
			0.24	0.6		$I_Q = 25\text{mA}$
Output leakage current	I_{QLEAK}			10	μA	
Output current limitation	I_{QLIMIT}	30	56	70	mA	internally limited & thermal shutdown
Output fall time	t_f	0.17	0.4	1	μs	1.2k Ω / 50pF, see Figure 2-3
Output rise time	t_r	0.4	0.5	1	μs	1.2k Ω / 50pF, see Figure 2-3
Output jitter ¹⁾	t_{QJ}		0.3	1	μs	For square wave signal with 1kHz
Delay time ²⁾	t_d	12	15	30	μs	see Figure 2-3
Power-on time ³⁾	t_{PON}		80	150	μs	$V_{DD} = 3\text{ V}$, $B \leq B_{RP} - 0.5\text{ mT}$ or $B \geq B_{OP} + 0.5\text{ mT}$
Chopper frequency	f_{OSC}		350		kHz	

- 1) Output jitter is the 1σ value of the output switching distribution
- 2) Systematic delay between magnetic threshold reached and output switching
- 3) Time from applying $V_{DD} = 3.0\text{ V}$ to the sensor until the output is valid

Table 3-5 Magnetic Characteristics

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
	B _{OP}	-40...170	10.3	15.0	19.8	mT	
	B _{RP}	-40...170	-19.8	-15.0	-10.3	mT	
	B _{HYS}	-40...170	22.5	30.0	37.5	mT	
Temperature compensation of magnetic thresholds	T _C			0		ppm/K	

Field Direction Definition

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.

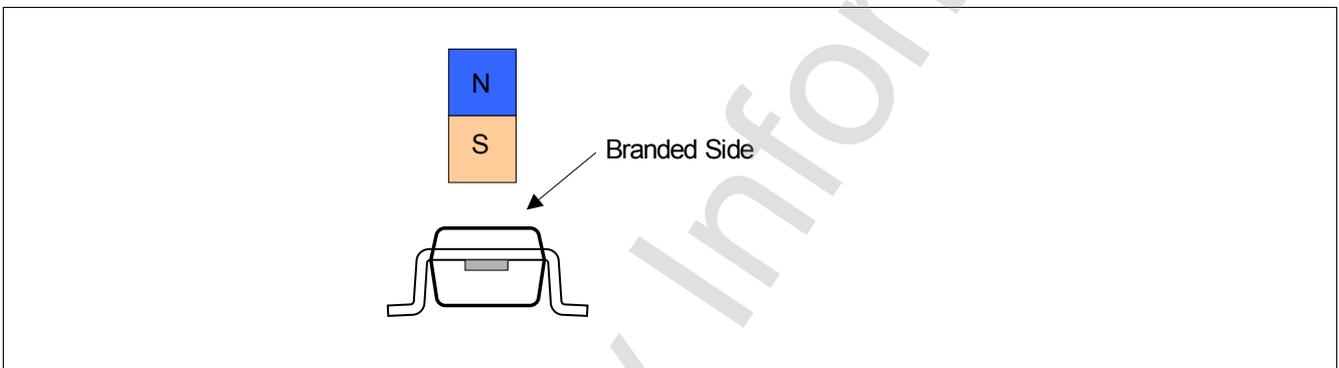


Figure 3-1 Definition of magnetic field direction

4 Package Information

The TLE4961-5 is available in the SMD package PG-SC59-3-5 with a SOT23 like pinout and footprint.

4.1 Package Outline PG-SC59-3-5

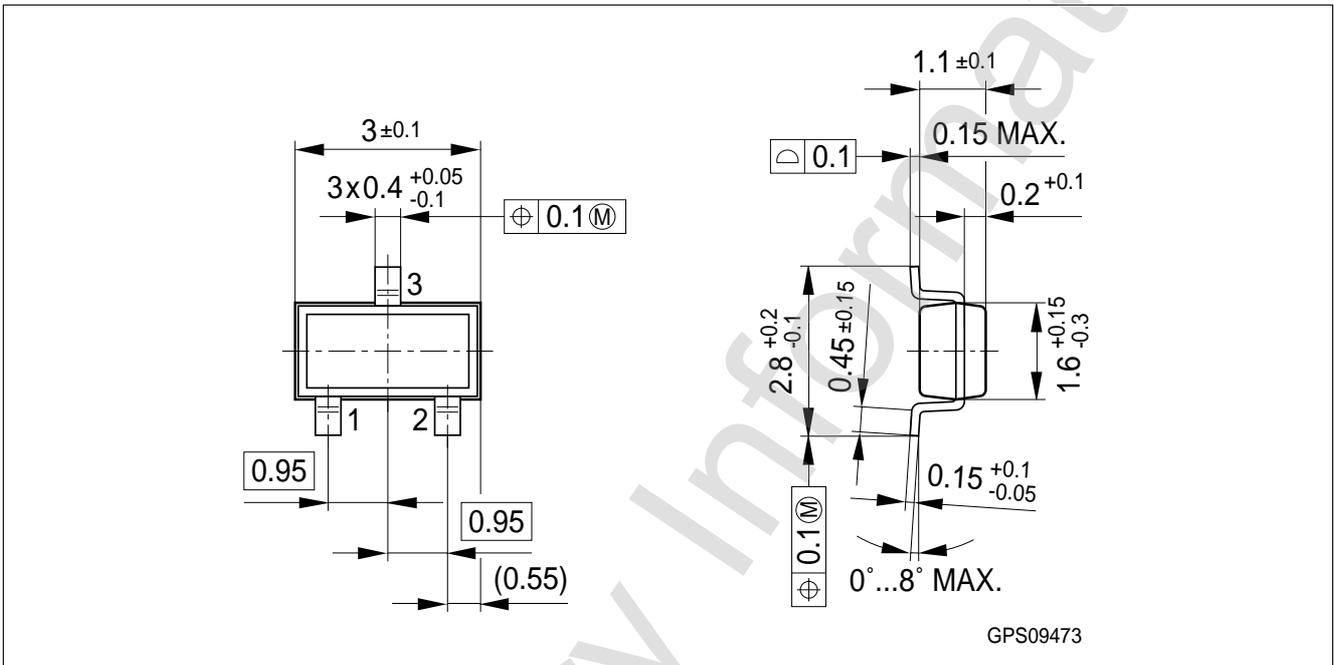


Figure 4-1 PG-SC59-3-5 Package Outline (All dimensions in mm)

4.2 Footprint

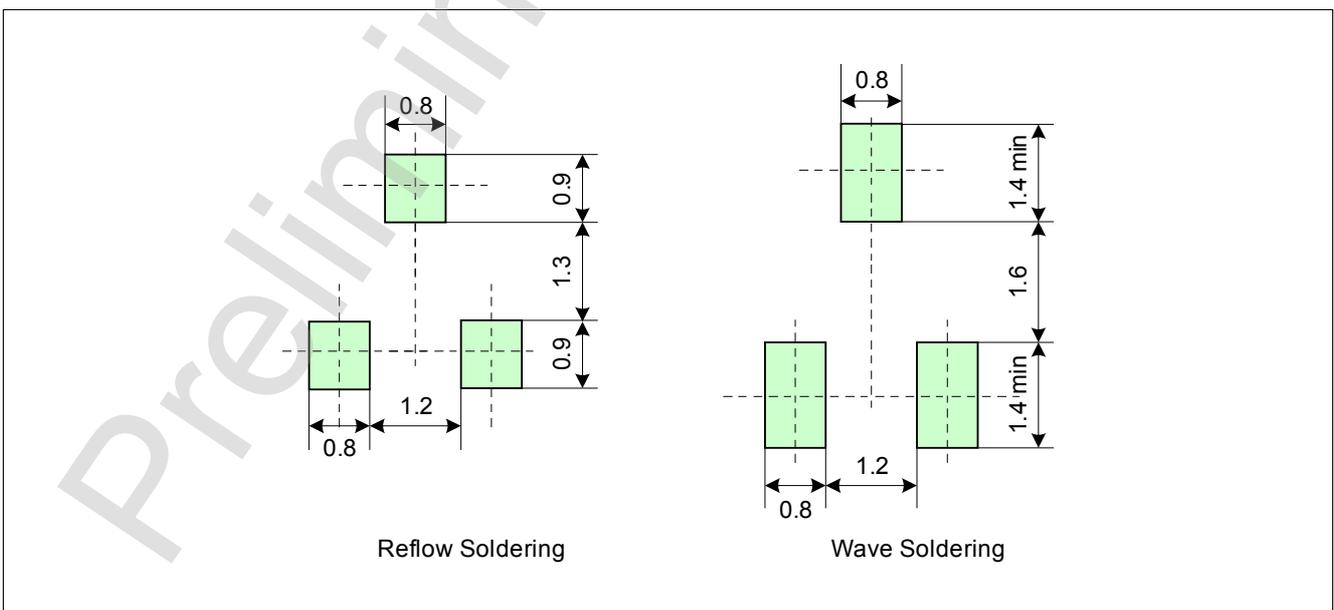


Figure 4-2 Footprint PG-SC59-3-5

4.3 Distance between Chip and Package

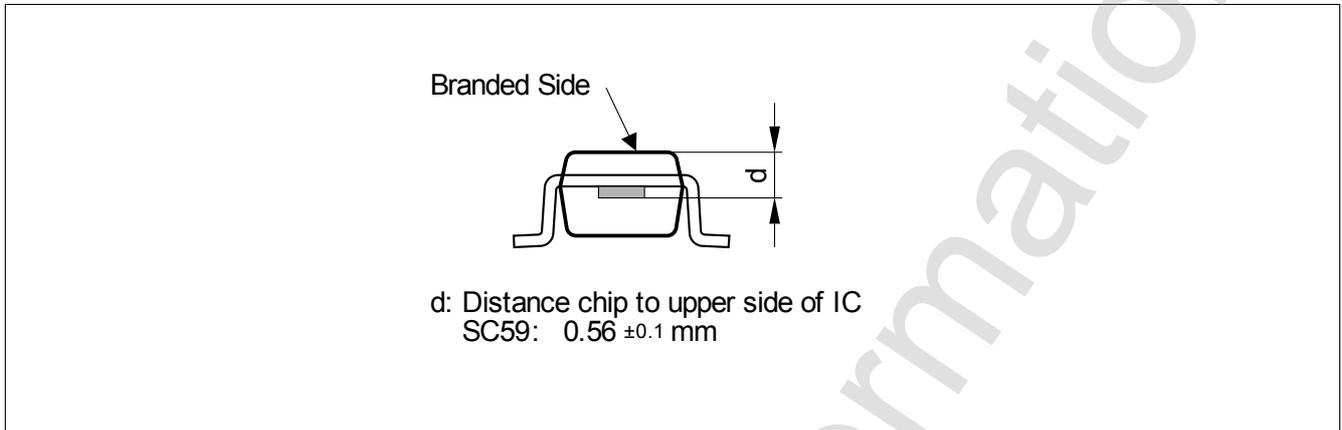


Figure 4-3 Distance between chip and package

4.4 Package Marking

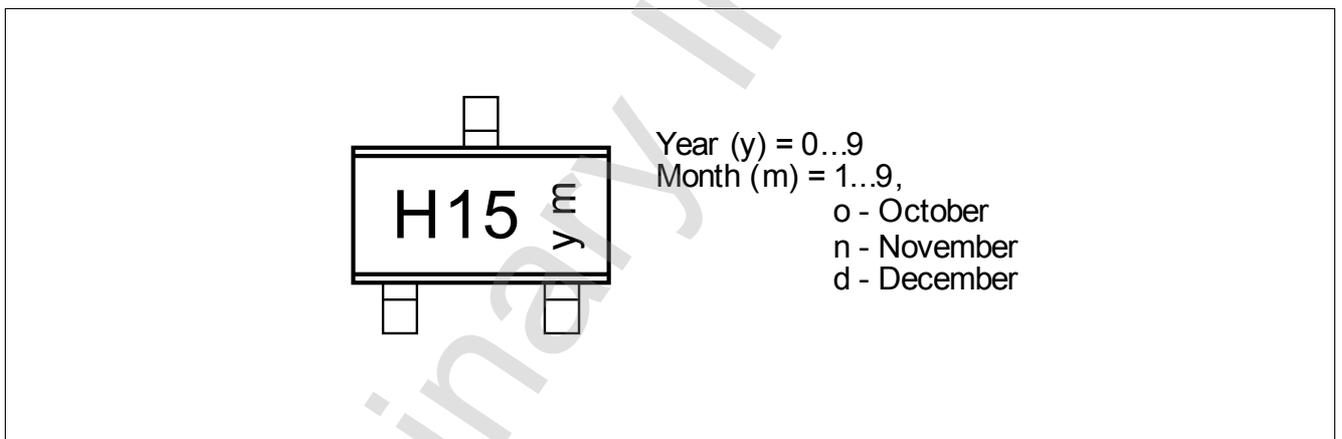


Figure 4-4 Marking of TLE4961-5

Preliminary Information

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